Increased Computer Peripheral Throughput By Using Data Available Withholding

Abstract of the Disclosure

A method and apparatus for a mutiprocessor system to simultaneously process multiple data write command issued from one or more peripheral component interface (PCI) devices by controlling and limiting notification of invalidated address information issued by one memory controller managing one group of multiprocessors in a plurality of mutiprocessor groups. The method and apparatus permits a multiprocessor system to almost completely process a subsequently issued write command from a PCI device or other type of computer peripheral device before a previous write command has been completely processed by the system. The disclosure is particularly applicable to multiprocessor computer systems which utilize non-uniform memory access (NUMA).